CLAIMS

What is claimed is:

1. A method comprising:

evaluating one or more source characters to determine whether each character will invert or maintain a current running disparity; and

determining a running disparity for each character before encoding the character based on the current running disparity and whether the character will invert or maintain the current running disparity.

2. The method of claim 1, wherein evaluating one or more source characters comprises evaluating each source character to determine a flip/hold bit based on whether the character will invert or maintain a current running disparity.

3. The method of claim 2, wherein determining a running disparity for each character comprises comparing the flip/hold bit of each character with the current running disparity.

4. The method of claim 3, wherein determining a running disparity for each character comprises using an exclusive or (XOR) function to compare the flip/hold bit with the current running disparity.

5. The method of claim 1, wherein evaluating one or more source characters comprises using a lookup table to determine whether each source character will invert or maintain the current running disparity.

6. The method of claim 1, wherein evaluating one or more source characters comprises using one or more logic gates to determine whether each source character will invert or maintain the current running disparity.

7. The method of claim 1, further comprising passing the current running disparity along with the associated source character to an encoder to encode the source character into a transmission character.

8. A circuit comprising:

a decoder to determine a flip/hold bit based on whether a source character will invert or maintain a current running disparity; and

a comparator coupled to the decoder to compare the flip/hold bit with the current running disparity to determine a running disparity for the source character before the source character is encoded.

9. The circuit of claim 8, wherein the comparator comprises one or more exclusive or (XOR) gates.

10. The circuit of claim 8, wherein the comparator comprises a pre-calculator to pre-calculate at least a portion of the running disparity.

11. The circuit of claim 10, wherein the pre-calculator comprises one or more exclusive or (XOR) gates.

12. The circuit of claim 8, further comprising an encoder coupled to the comparator to receive the current running disparity and the associated source character and to encode the source character to a transmission character.

13. The circuit of claim 12, wherein the encoder is an 8B/10B encoder that does not contain disparity calculation circuitry.

14. An apparatus comprising:

means for evaluating one or more source characters to determine a flip/hold bit based on whether each source character will invert or maintain a current running disparity; and

means for comparing the flip/hold bit of each source character with the current running disparity to determine a running disparity for each source character before the source character is encoded.

15. The apparatus of claim 14, wherein the means for comparing the flip/hold bit with the current running disparity comprises one or more exclusive or (XOR) gates.

16. The apparatus of claim 14, wherein the means for comparing the flip/hold bit with the current running disparity comprises means for pre-calculating at least a portion of the running disparity.

17. The apparatus of claim 14, wherein the means for evaluating the one or more source characters comprises one or more lookup tables.

18. The apparatus of claim 14, wherein the means for evaluating the one or more source characters comprises one or more logic gates to determine whether each source character will invert or maintain the current running disparity.

19. The apparatus of claim 14, further comprising an encoder coupled to the comparing means to receive the running disparity and the associated source character and to encode the source character to a transmission character.

20. The apparatus of claim 19, wherein the encoder is an 8B/10B encoder that does not contain disparity calculation circuitry.